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(54) Title: NEW METHOD OF FORMING FINE CIRCUIT LINES

(57) Abstract

A new method of forming circuit lines on a substrate by applying conductive metal(s) using copper foil as a carrier. The copper foil is etched away, leaving the conductive metals embedded in the surface of the substrate. A photoresist is used to expose trenches which define the desired circuit and copper is applied onto the exposed conductive metals. The method is particularly suited to manufacturing the outer layers of multi-layer circuit boards.

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NEW METHOD OF FORMING FINE CIRCUIT LINES

Priority is claimed from United States Provisional Patent Application No. 60/016,665 filed on May 1, 1996.

This invention relates generally to methods for producing printed circuit boards. In particular, it relates to a new method of forming very fine circuit lines.

In the typical production of printed circuit boards, thin copper foil is laminated to an insulating substrate, most often a glass reinforced epoxy resin prepreg, and then that laminate is further processed to convert the copper foil into a circuit pattern by selectively removing portions of the copper by chemical etching. Such etching is generally satisfactory, but its limitations become apparent whenever finer (narrower) circuit lines are required.

Quite frequently, the copper foil may be treated prior to lamination in order to enhance its ability to bond to the insulating substrate. For purposes of this application, unless otherwise specified, references herein to copper foil shall be construed as referring interchangeably to both treated and untreated copper foil.

In practice, the etchants do not create vertical sides of the circuit lines. Instead, they tend to etch away too much copper at the top of the line by undercutting the resist and less at the bottom of the line, leaving a somewhat rapezoidal-shaped circuit line. As a result, the minimum width of the circuit lines is limited by the need to allow for such non-uniform etching. This problem was discussed in US 5,437,914 and it was shown that the shape of the etched circuit lines was affected by the shape of the grain structure of the copper foil. Improved accuracy of etching was to be obtained according to the '914 patent by laminating the copper foil to the substrate with the "shiny" side down, which is contrary to the conventional practice. An improved etching factor was obtained, indicating that the sides of the circuit lines were more nearly vertical.

Another approach to improving the accuracy of circuit lines is to use thinner copper foils, since they can be etched quickly with less undercutting. However, such foils are not easy to handle. Consequently, it has been proposed to deposit thin layers of copper on supporting sheets which can be removed after the

needed in the circuit design. The remaining copper layer is turned into the conductive circuit lines by conventional etching procedures.

The process of the present invention is clearly different from conventional circuit board processing in which the circuit lines are formed by selectively etching copper away. As explained above, chemical etching has inherent limitations which become particularly troublesome as circuit lines become narrower and their pitch closer. The new process of the invention deposits the circuit lines directly into spaces created by the use of a photoresist, which leaves open trenches to be filled by electrodeposition of copper. This is made possible by the conductive layer which remains on the surface of the substrate once the covering copper foil carrier has been removed. The process of the invention is also different from that of the Ohmega process in which the layer at the surface of the substrate serves as a resistor.

The process is shown in the block diagram of Figure 1 as applied to the outer layers of a multi-layer board. In the first step, copper foil is passed through a bath of soluble compounds of the conductive metals and they are electrodeposited to a thickness of about 0.2 to 5 μm on one surface of the foil, either the matte or shiny side. As previously identified, either before or after application of the conductive metal, the copper foil may be given a treatment (such as nodular copper) to improve its adhesion to the insulating substrate. The metals or alloys may be tin, nickel, tin-zinc, zinc-nickel, tin-copper and others, provided that they are resistant to the etchant used to remove copper during a subsequent step. The conditions of the electrodeposition process are typical of those used commercially to provide protective metal coatings on copper foil.

In the second step the coated copper foil is laminated to an insulating substrate, such as the commonly used glass reinforced epoxy resins, using conventional techniques and with the conductive metals next to the substrate.

The next step is to etch away the copper foil, leaving the thin layer of conductive metal embedded in the surface of the substrate. For this purpose, the etchant is selected from those which will remove copper, but not the metals of the conductive layer to a significant extent. An example of such etchants is

ammoniacal cupric chloride. Thin copper foils have been applied in the past from aluminum supporting layers, with the aluminum being etched away in a similar manner. It is an advantage of the present process that copper is recoverable and that contamination with dissolved aluminum is avoided, which would occur if aluminum were to be substituted for copper in the process of the invention. Once the copper has been etched away the conductive metal (or alloy) layer is exposed and ready for application, imaging, and curing of the photoresist.

In the process of this invention, the uncured photoresist is removed to expose trenches which will form the circuit lines. It will be evident to those skilled in the art that cured photoresist will more accurately define the circuit lines and that the copper which fills the trenches will more closely approach the ideal rectangular shape than would circuit lines formed by etching away copper in exposed areas. This means that finer circuit lines can be made because their shape is not determined by an etching process. Consequently, rather than 4 mil (100 μm) lines and spaces, the new process permits reducing the lines and spaces to about 1 mil (25 μm).

The copper is electrodeposited using conventional procedures such as are often used to plate copper onto the outside of multilayer circuit boards. It is possible to do this when the thin layer of metals embedded in the surface of the substrate is sufficiently conductive. If not, electroless plating of copper can be used to facilitate the electrodeposition of the circuit lines. The copper can be built up in thickness as desired, up to the height of the photoresist which defines the shape of the trenches. Conventional electrodeposition conditions will be used.

At this point, the circuit lines have been formed. What remains is to remove the photoresist by conventional means, following which the conductive metal layer which has been exposed is removed by using an etchant, such as acid cupric chloride or sulfuric peroxide.

It will be readily apparent to those skilled in the art that the specific steps of the invention (*e.g.* those illustrated in Figure 1) may be performed in any order that is commercially practicable. In particular, the steps subsequent to applying the

conductive metal to the laminate may be performed in whatever method is feasible for the operator.

The invention has particular value in making the outer layers of multi-layer circuit boards. Multilayer circuit boards generally have holes connecting outer with inner layers which are electroless plated with copper and then the circuit lines are formed by electroplating. The typical procedure is shown in the block diagram of Figure 2. Copper foil is laminated with an intervening layer of prepreg to the inner circuit layers, but is not etched away. Electroless plating is used to deposit copper over the foil and down the holes which connect the layers. Then, a resist is applied and the copper circuit lines are electrodeposited. At this point, the excess copper foil must be removed by etching. However, the circuit lines and the plated holes must be protected by a step of electrodepositing a resistant metal, such as tin. Then the resist can be removed and the exposed copper foil etched. It can be appreciated that such a step causes the sides of the circuit lines not protected by the tin to be attached also. In the present invention, tin need not be applied since it is only necessary to remove the thin conductive layer, which can be accomplished very quickly. Importantly, the substantial costs of disposing of solutions needed for applying and removing the tin layer are avoided.

Figure 3 illustrates the circuit lines formed in the outer layers of multi-layer circuit boards by conventional etching processes, compared to the essentially rectangular line formed using the process of the invention. The circuit lines of the prior art are severely undercut by the need to etch away copper foil after the circuit lines are formed (the top being protected by the tin coating).

The process of the invention makes possible more accurate production of circuit lines and thus, the circuit designer does not have to compensate for the inaccuracy inherent in the formation of circuit lines by etching. This means the resulting circuit can be smaller and more compact. The process uses techniques which are familiar to circuit board manufacturers and does not involve large changes in technology. In fact, it is expected that the production processes will be simplified when the process of the invention is adopted.

CLAIMS

1. A method of forming circuit lines comprising the steps of
   (a) applying on a sheet of copper foil a layer of conductive metals resistant to etchants used to remove copper;
   (b) laminating the conductive metal containing sheet of copper foil of (a) with a prepreg or a film substrate;
   (c) etching away the copper foil from the laminate produced in (b) and leaving the conductive metal(s) embedded in the surface of said prepreg or film substrate;
   (d) applying, imaging, and curing a photoresist over the conductive metal(s) and substrate produced in (c);
   (e) removing the uncured photoresist of (d) leaving trenches having exposed conductive metal(s);
   (f) applying copper onto the exposed conductive metals of (e) to produce circuit lines;
   (g) removing the cured photoresist of (d) to expose conductive metal(s) and etching away the exposed conductive metals, thereby producing a circuit on said substrate.

2. The method of Claim 1 wherein said layer of conductive metal is 0.2 to 5 µm thick.

3. The method of Claim 1 wherein the conductive metals are applied to the copper foil by electrolytic deposition.

4. The method of Claim 1 wherein the conductive metals are applied to the copper foil by chemical vapor deposition.

5. The method of Claim 1 wherein the conductive metals are applied to the copper foil by electroless deposition.

6. The method of Claim 1 wherein the conductive metals are applied to the copper foil by sputtering.

7. The method of Claim 1 wherein said conductive metals are selected from the group consisting of tin, nickel, tin-zinc, zinc-nickel, and tin-copper.

Figure 2

PRIOR ART

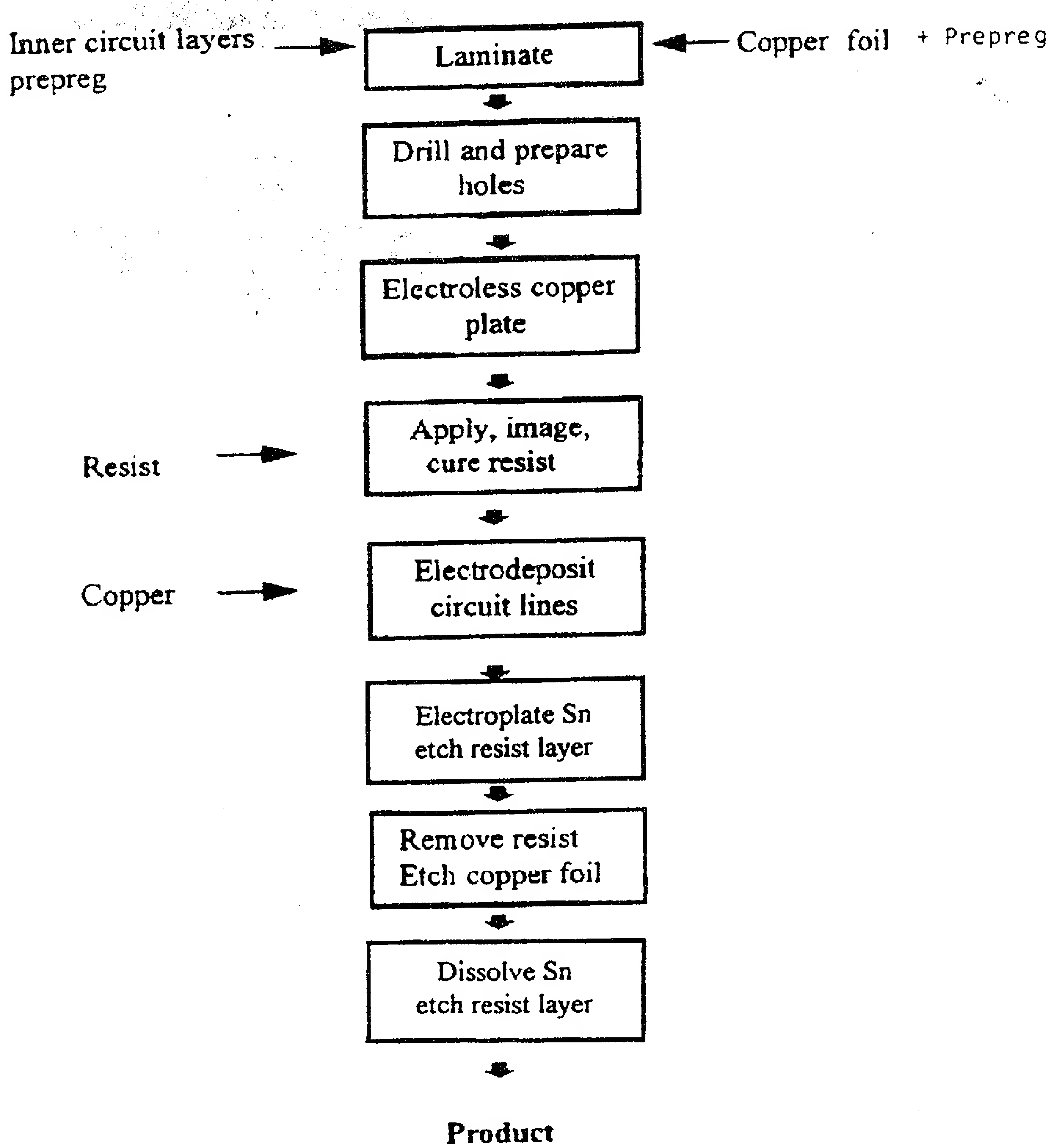
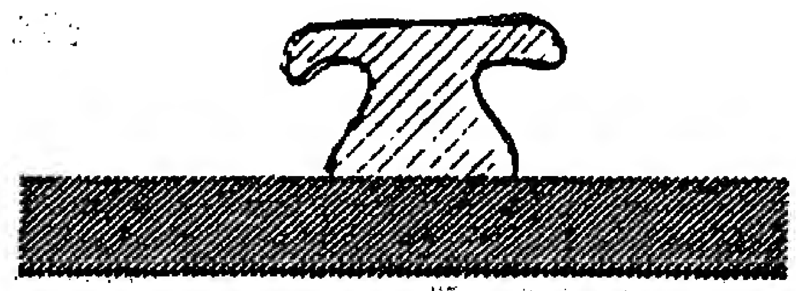
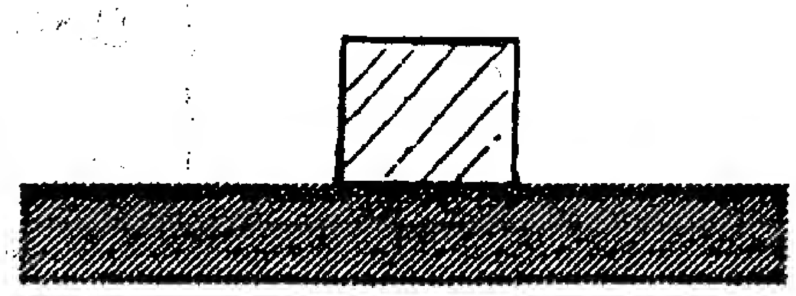


FIGURE 3



Prior Art



Invention

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H05K3/02 H05K3/10

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 017 271 A (WHEWELL ET AL.) 21 May 1991 see the whole document	1-3,5-8, 10
X	PATENT ABSTRACTS OF JAPAN vol. 13, no. 371 (E-807), 17 August 1989 & JP 01 124286 A (HITACHI CHEM CO), 17 May 1989, see abstract	1,7,8,10
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 181 (E-750), 27 April 1989 & JP 01 008694 A (HITACHI CHEM CO), 12 January 1989, see abstract	1,5,7,8, 10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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rmation on patent family members

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